# Appendix

## A. Model Linearization

In this section, the expressions are transformed into mixed integer linear form with linearization technique.

(7) can be transformed into the following formulation.

 (A1)

(20) can be transformed into the following formulation.

 (A5)

## B. Detailed Analysis of the Constraints

For (14), the logical constraints between line status in PI stage (*zij*,*PI*) and RI stage (*zij*,*RI*,*c*) are affected by binary variable *x*RCS *ij* and the binary value of *FL ij,c* and *FRCS ij,c*. Regarding the combination of line faults and switch faults, the following four situations are discussed.

Case 1: Both line *ij* and RCS at branch *ij* experience a fault, i.e., *FL ij,c*=1 and *FRCS ij,c*=1. In this case, (14) is converted to (B1). Apparently, line *ij* have to be opened at RI stage.

 (B1)

Case 2: The line *ij* experience a fault while the switch on line *ij* is functional, i.e., *FL ij,c*=1 and *FRCS ij,c*=0. In this case, (14) is converted to (B2). RCS cannot effectively operate on the damaged line and the line *ij* is still opened.

 (B2)

Case 3: The line *ij* is normal, but switch at line *ij* experience a fault, i.e., *FL ij,c*=0 and *FRCS ij,c*=1. In this case, (14) is converted to (B3). RCS at line *ij* cannot be operated to stop the propagation of the fault.

 (B3)

Case 4: Both line *ij* and switch at line *ij* are normal, i.e., *FL ij,c*=0 and *FRCS ij,c*=0. In this case, (14) is converted to (B4). If line *ij* is deployed with switch, the propagation of a fault can be prevented in RI stage.

 (B4)

For (15a)(15b), the logical relationship between the line status at PI stage (*zij*,*PI*) and the fault status of nodes at both two ends of the line in RI stage (*fi*,*c*,*RI*) are affected by the binary value of *FL ij,c* and *FRCS ij,c*. Regarding the combination of line faults and switch faults, the following four situations are discussed.

Case 1: Both line *ij* and RCS at branch *ij* experience a fault, i.e., *FL ij,c*=1 and *FRCS ij,c*=1. In this case, (15a)(15b) are converted to (B5)(B6). If the line is opened at the pre-disaster phase, the fault will not be transmitted. If the line is closed before the disaster, the fault will extend from branch to node.

 (B5)

 (B6)

Case 2: The line *ij* experience a fault while the switch on line *ij* is functional, i.e., *FL ij,c*=1 and *FRCS ij,c*=0. In this case, (15a)(15b) are converted to (B7)(B8). The analysis is divided into three situations. (i) If the line is opened at the pre-disaster phase, the fault will not be transmitted. (ii) If the line is closed at the pre-disaster phase, and the line is installed with a switch, then the fault could be interrupted by the switch. (iii) If the line is closed at the pre-disaster phase, and there is no switch install on the line, then the fault will extend from branch to node.

 (B7)

 (B8)

Case 3: The line *ij* is normal, but switch at line *ij* experience a fault, i.e., *FL ij,c*=0 and *FRCS ij,c*=1. In this case, (15a)(15b) are converted to (B9)(B10). Since the line is normal, the fault status will not be propagated.

 (B9)

 (B10)

Case 4: Both line *ij* and switch at line *ij* are normal, i.e., *FL ij,c*=0 and *FRCS ij,c*=0. In this case, (15a)(15b) are converted to (B11)(B12). Since the line is normal, the fault status will not be propagated.

 (B11)

 (B12)

For (17), the logical constraints between switch status in RI stage (*zij*,*RI*,*c*) and SR stage (*zij*,*SR*,*c*) are affected by *FL ij,c* and *FRCS ij,c*. Regarding the combination of line faults and switch faults, the following four situations are discussed.

Case 1: Both line *ij* and RCS at branch *ij* experience a fault, i.e., *FL ij,c*=1 and *FRCS ij,c*=1. In this case, (17) is converted to (B13). Apparently, line *ij* have to be opened at RI stage.

 (B13)

Case 2: The line *ij* experience a fault while the switch on line *ij* is functional, i.e., *FL ij,c*=1 and *FRCS ij,c*=0. In this case, (17) is converted to (B14). Apparently, line *ij* have to be opened at RI stage.

 (B14)

Case 3: The line *ij* is normal, but switch at line *ij* experience a fault, i.e., *FL ij,c*=0 and *FRCS ij,c*=1. In this case, (17) is converted to (B15). Due to switch faults, the line status at RI stage is unchanged from SR stage.

 (B15)

Case 4: Both line *ij* and switch at line *ij* are normal, i.e., *FL ij,c*=0 and *FRCS ij,c*=0. In this case, (17) is converted to (B16). With the functional switch, the line status of the line at SR stage is determined by the overall network topology for minimization of load loss.

 (B16)

## C. Flow chart of scenario-based distributionally robust optimization

The overall process of scenario-based distributionally robust optimization is shown in Fig.1.

Firstly, initialize the upper bound UB and lower bound LB of the problem. Then, iteratively solve MP and SP to update UB and LB until the convergence gap is met. The iteration loop process is summarized as follows. Solve MP(25) to obtain ***X****l*\*, *Cl I*\* and *αl\**. With *Cl I*\* and *αl\**, LB can be updated. And with the determined ***X****l*\*, solve c-SSP(27) to obtain *Cl R,c*\*. Then, with *Cl R,c*\*, solve (28) to obtain *Q*(***X****l*\*) and Pr*l c*\*. With *Q*(***X****l*\*), UB can be updated. After completing each iteration, check if the gap meets the required condition. If the gap meets the required condition, then end the loop and output the optimal switch deployment strategy. If the gap still does not meet the required condition, new variables *Yl c* and new constraints (25c)(25d) are added with Pr*l c*\*.



Fig. 1. The overall model solving process flow chart